Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for the processing of an electromagnetic input signal comprising the steps of:

producing a bounded phase signal that is an n-bit 2's compliment number in the range of [-1, 1] from said input signal; and

producing an unwrapped phase difference signal from said bounded phase signal.

2. (Original) The method of Claim 1, wherein said bounded phase signal is produced by using a CORDIC processor to produce a wrapped phase signal that is an n-bit 2's compliment number in the range of [-1, 1] as said bounded phase signal.

3. (Original) The method of Claim 2, wherein said unwrapped phase difference signal is produced by taking a 2's compliment subtraction using said bounded phase signal.

4. (Original) The method of Claim 1, further comprising the step of correcting said bounded phase signal to produce a corrected phase signal.

5. (Original) The method of Claim 4, wherein said bounded phase signal is a wrapped phase signal that is an n-bit 2's compliment number in the range of [-1, 1] and said corrected phase signal is produced by taking a 2's complement addition using said bounded phase signal, wherein said phase difference signal is produced using said corrected phase signal.

6. (Currently Amended) A method for processing sample information for an input signal to generate a phase signal from an unwrapped phase difference signal for inputting into a phase modulator, said method comprising the steps of:

receiving said sample information;

scaling said sample information and producing a wrapped phase signal that is an n-bit 2's compliment number in the range of [-1, 1] for said sample; and

determining said unwrapped phase difference signal by:

determining the difference between said wrapped phase signal and another wrapped phase signal produced from a previous sample and producing a wrapped phase difference signal; and

wherein said unwrapped phase difference signal is said wrapped phase difference signal when said wrapped phase difference signal is less than or equal to π, and said unwrapped phase difference signal is said wrapped phase difference

signal plus the sign of said another wrapped phase signal multiplied by 2π otherwise.

7. (Currently Amended) The method of Claim 6, wherein said wrapped phase signal is ~~an n-bit 2's compliment number in the range of [-1, 1]~~ produced by using a CORDIC processor.

8. (Original) The method of Claim 7, wherein said unwrapped phase difference signal is produced by taking a 2's compliment subtraction using said wrapped phase signal.

9. (Original) The method of Claim 6, further comprising the step of correcting said wrapped phase signal to produce a corrected phase signal.

10. (Original) The method of Claim 9, wherein said wrapped phase signal is an n-bit 2's compliment number in the range of [-1, 1] and said corrected phase signal is produced by taking a 2's complement addition using said wrapped phase signal, and wherein said unwrapped phase difference signal is produced using said corrected phase signal.

11. (Original) The method of Claim 6, wherein said sample information is in the form of one or more selected from the group consisting of in-phase and quadrature information and magnitude and phase information.

12. (Original) A method for processing sample information for an input signal to generate a phase signal from an unwrapped phase difference signal for inputting into a phase modulator, said method comprising the steps of:

receiving said sample information;

determining an n-bit 2's compliment number in the range of [-1, 1] from said sample information and producing a wrapped phase signal for said sample; and

determining said unwrapped phase difference signal by taking a 2's compliment subtraction using said wrapped phase signal.

13. (Original) The method of Claim 12, wherein said wrapped phase signal produced by using a CORDIC processor.

14. (Original) The method of Claim 12, further comprising the step of correcting said wrapped phase signal to produce a corrected phase signal.

15. (Original) The method of Claim 14, wherein said corrected phase signal is produced by taking a 2's complement addition using said wrapped phase signal, and wherein said unwrapped phase difference signal is produced using said corrected phase signal.

16. (Original) The method of Claim 12, wherein said sample information is in the form of one or more selected from the group consisting of in-phase and quadrature information and magnitude and phase information.

17. (Currently Amended) An apparatus for processing an electromagnetic input signal comprising processing circuitry producing a bounded phase signal using an n-bit 2's compliment number in the range of [-1, 1] from said input signal and producing an unwrapped phase difference signal from said bounded phase signal.

18. (Canceled).

19. (Original) The apparatus of Claim 17, wherein said processing circuitry produces said unwrapped phase difference signal by taking a 2's compliment subtraction using said bounded phase signal.

20. (Original) The apparatus of Claim 17, wherein said processing circuitry further comprises circuitry for correcting said bounded phase signal to produce a corrected phase signal.

21. (Currently Amended) The ~~method~~ apparatus of Claim 20, wherein said bounded phase signal is an n-bit 2's compliment number in the range of [-1, 1] and said processing circuitry produces said corrected phase signal by taking a 2's complement addition using said bounded phase signal, wherein said phase difference signal is produced using said corrected phase signal.

22. (Original) The apparatus of Claim 17, wherein said processing circuitry includes one or more digital signal processors incorporating a CORDIC processor.

23. (Original) The apparatus of Claim 22, wherein said digital signal processors is located on an ASIC chip.

24. (Original) A signal transmitter comprising:

baseband processing circuitry for processing an input signal to generate sample information containing amplitude and phase sample information for said input signal;

phase processing circuitry for receiving said phase sample information determining a wrapped phase signal for said phase sample information using an n-bit 2's

compliment number in the range of [-1, 1]; determining an unwrapped phase difference signal by taking a 2's compliment subtraction using said wrapped phase signal and another wrapped phase signal from previous phase sample information; determining a phase signal from said unwrapped phase difference signal;

phase modulating circuitry for modulating a carrier wave using said phase signal to produce a phase modulated signal; and

amplifying circuitry for regulating said phase modulated signal using said amplitude sample information to generate an output signal for transmission by said transmitter.

25. (Original) The transmitter of Claim 24, wherein said phase processing circuitry produces a corrected phase signal by taking a 2's complement addition using said wrapped phase signal, wherein said unwrapped phase difference signal is produced using said corrected phase signal.

26. (Currently Amended) The ~~apparatus~~ transmitter of Claim 24, wherein said phase processing circuitry includes one or more digital signal processors incorporating a CORDIC processor.

27. (Currently Amended) The ~~apparatus~~ transmitter of Claim 26, wherein said digital signal processors is located on an ASIC chip.

28. (Currently Amended) The ~~apparatus~~ transmitter of Claim 24, wherein said phase modulating circuitry includes a sigma delta modulator and a phase locked loop to modulated said carrier wave using said phase signal.

29. (Currently Amended) The ~~apparatus~~ transmitter of Claim 24, wherein said amplifying circuitry comprises a plurality of segments.

30. (Currently Amended) The ~~apparatus~~ transmitter of Claim 29, wherein one or more of said segments is independently controlled as a power amplifier by at least a portion of said amplitude sample information to contribute power to said output signal.

31. (Currently Amended) The ~~apparatus~~ transmitter of Claim 30 further comprising a combining circuit for combining said power from said segment to generate said output signal, said combining circuit comprising one or more selected from the group consisting of power transformers, quarter-wave transmission lines, discrete LC components, and a Pi-networks.

32. (Currently Amended) The ~~apparatus~~ transmitter of Claim 29, wherein one or more of said segments is independently controlled as a current source by at least a portion of said amplitude sample information to contribute current to an output signal.